ABSTRACT OF THE INVENTION

A system and method provides a pulse train clock signal having a portion appropriate for loading and loading a scan chain of a circuit under test, and a higher frequency portion with a sharp leading edge appropriate for inputting a test signal into the scan elements for transition fault testing. The circuit and method provide this signal by taking as inputs to a multiplexer switch, two synchronous pulse trains, and provide edge sharpening and frequency raising to one of the signals, and input each of these signals into a multiplexer switch, and rapidly switch between these signals depending upon a selection control signal that is synchronous with each signal. The multiplexer switches between these input signals during a low valued portion of each signal so that the less sharp edge of the selection control signals and the high frequency input signal do not affect the sharp pulse of the very high frequency portion. An embodiment of the invention includes both a static low signal input top the multiplexer for transition switching, and special alignment circuits to compensate for the different delays experienced by each of the inputs and selection signals.